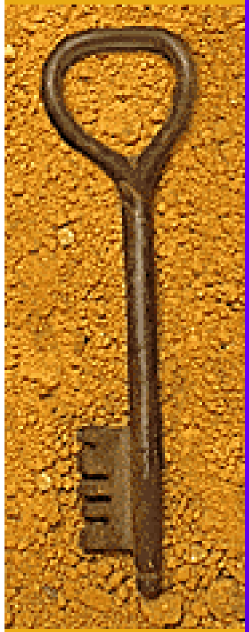

VietNam 2006

Nanopillars Transistor for 300 K Applications

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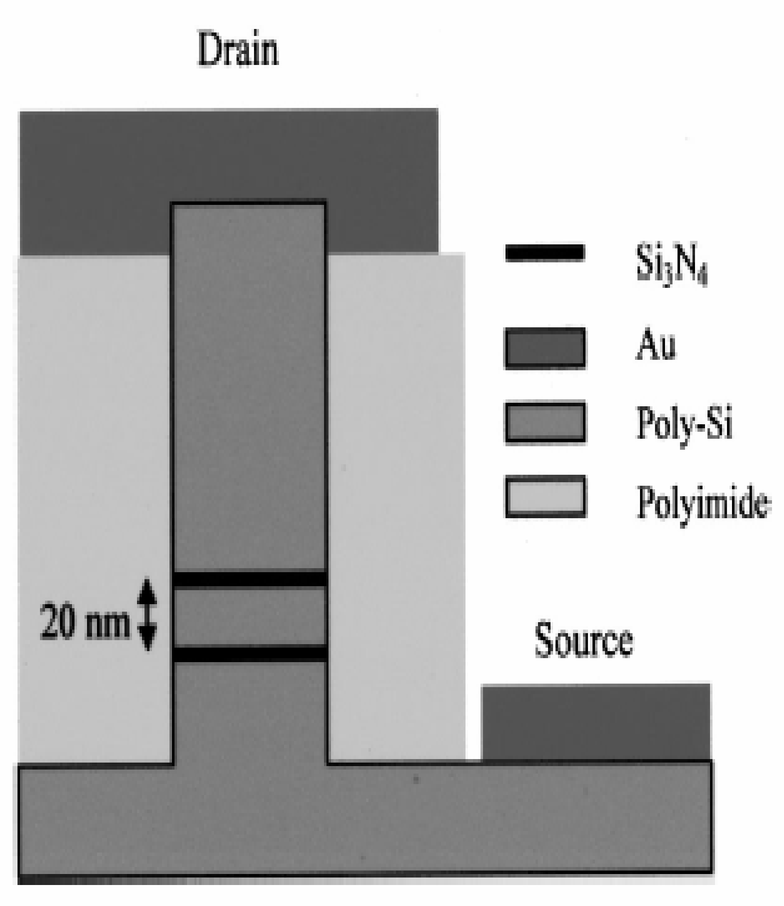
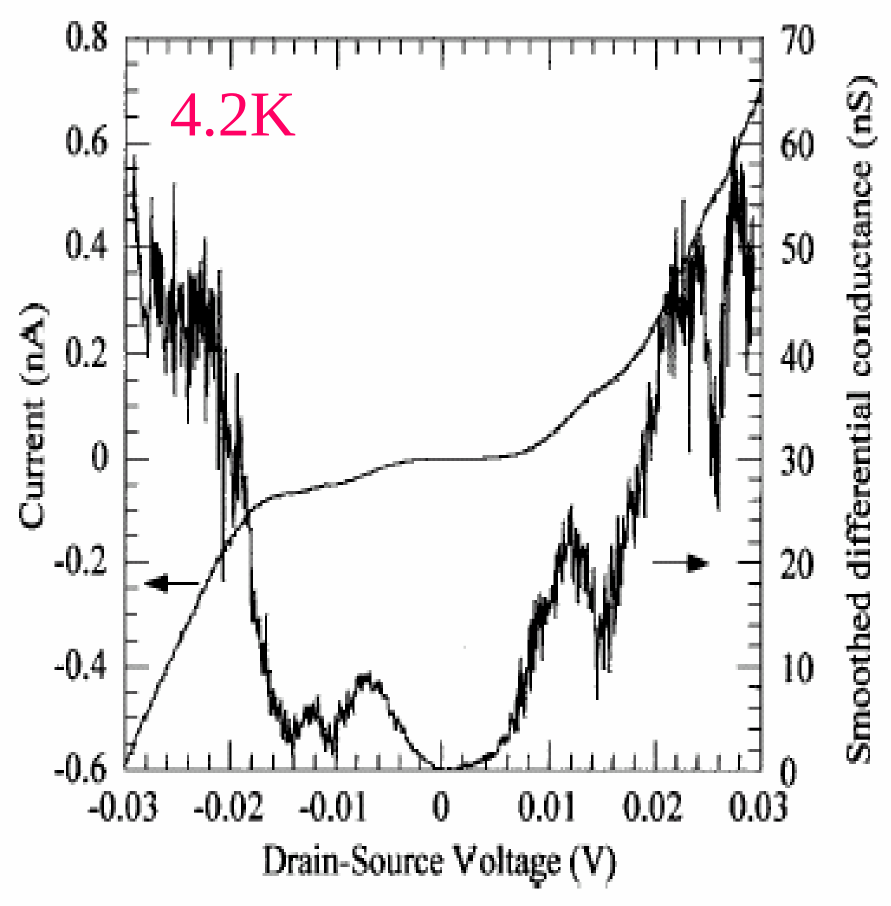
Criterions for RTSET

- The hunt for - no cooling required - SET has been more than two decades
- CMOS processing compatible
- Distinct I-V characteristics
- Low voltage operation

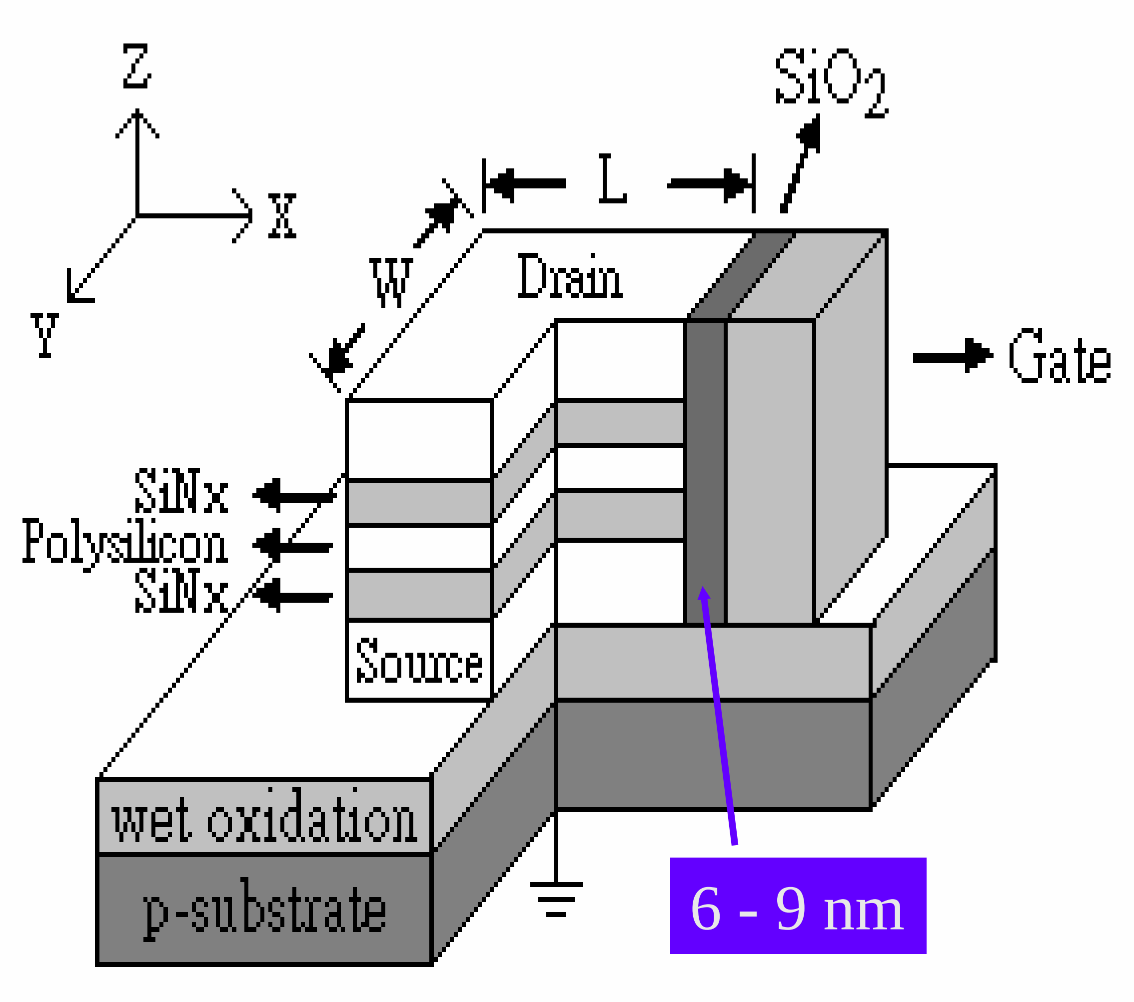
Si/SiNx/Si structure



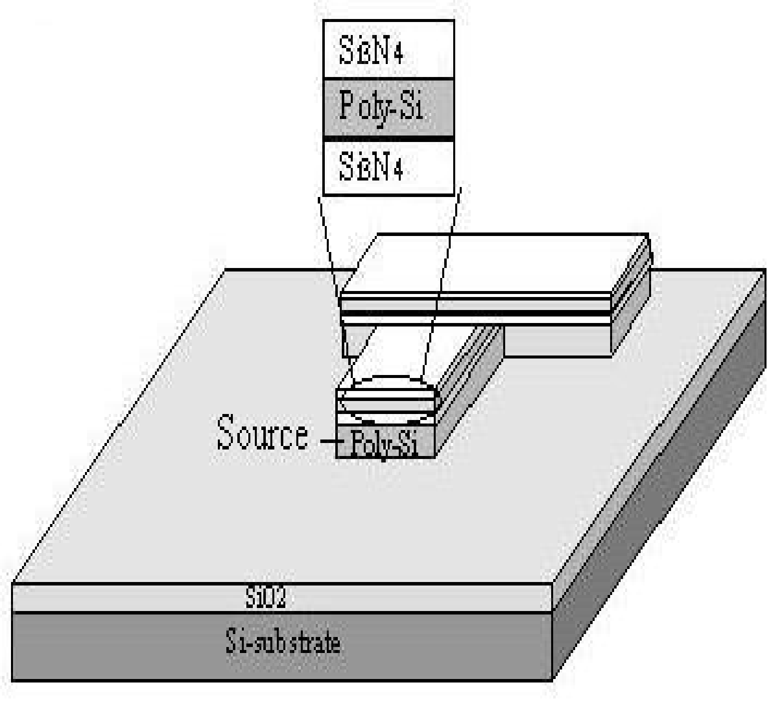


D. M. Pooley, and H. Ahmed, APL 74, 2191(1999)

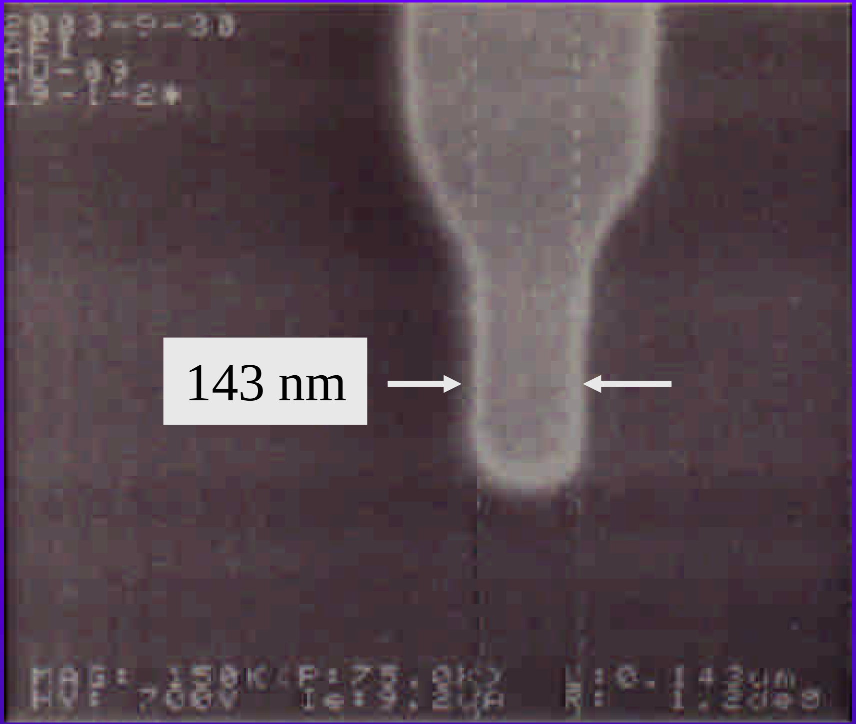
Our transistor



Source electrode

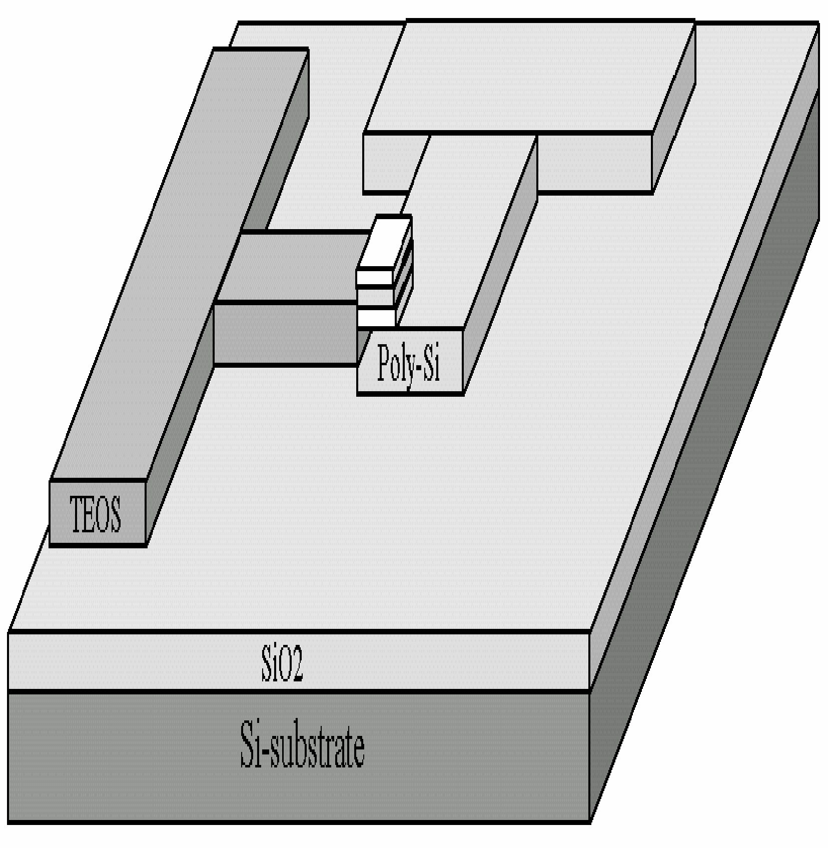


(a) P-type silicon substrate is prepared,and wet oxidation grew 200 nm oxide then deposition 200 nm polysilicon(*in-situ* phosphorous)、3 nm Si3N4、3 nm polysilicon、3 nm Si3N4,and defined source region of 140 nm width .

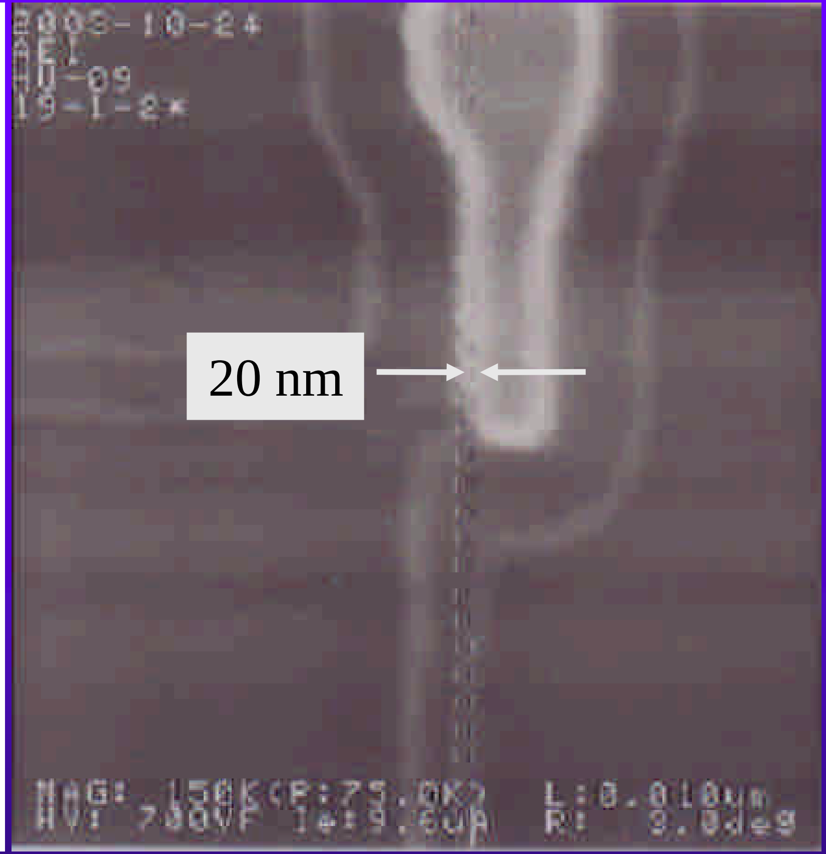


(1) mask1 by In-Line SEM

Define a fine tip

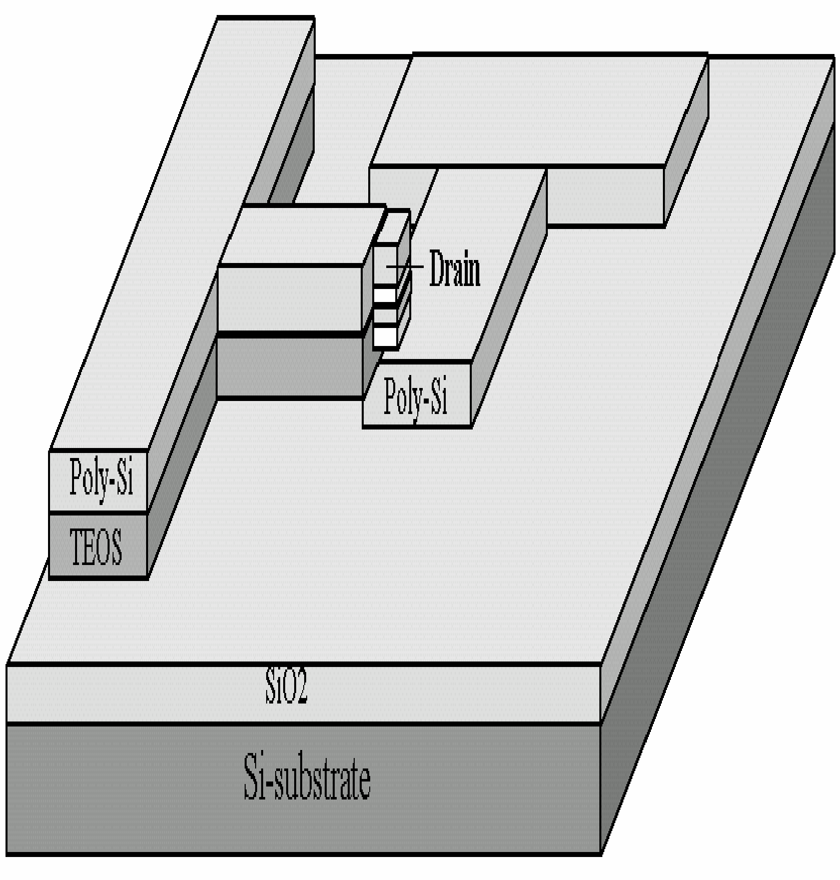


(b) Deposition 200 nm TEOS ,and defined active region of 10 nm width.

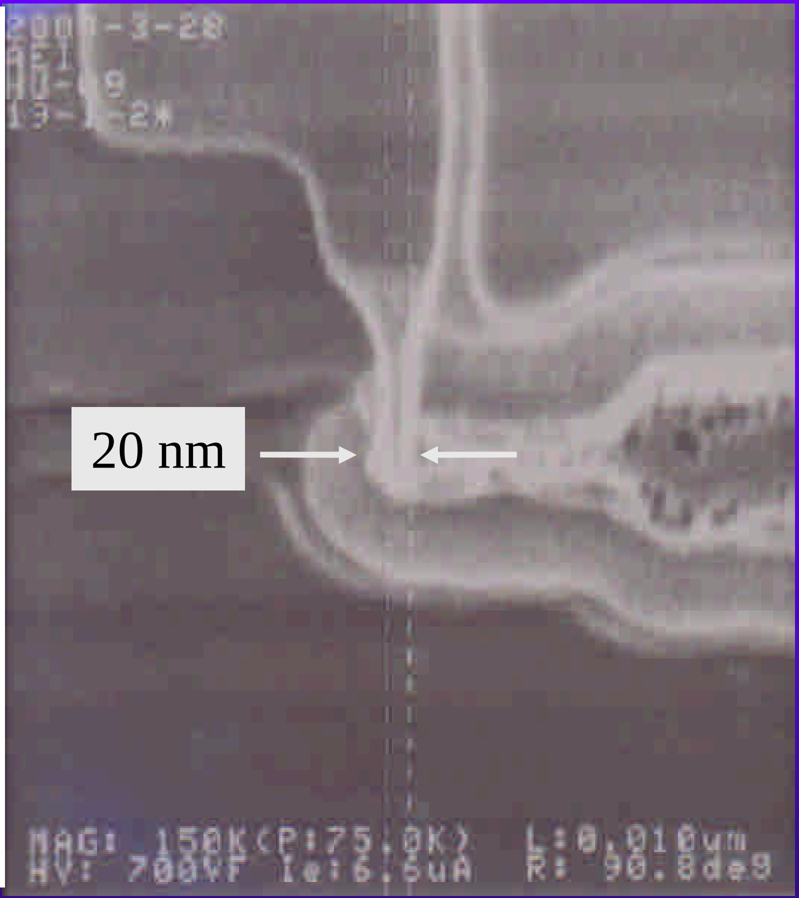


(2) mask2 by In-Line SEM

Drain electrode

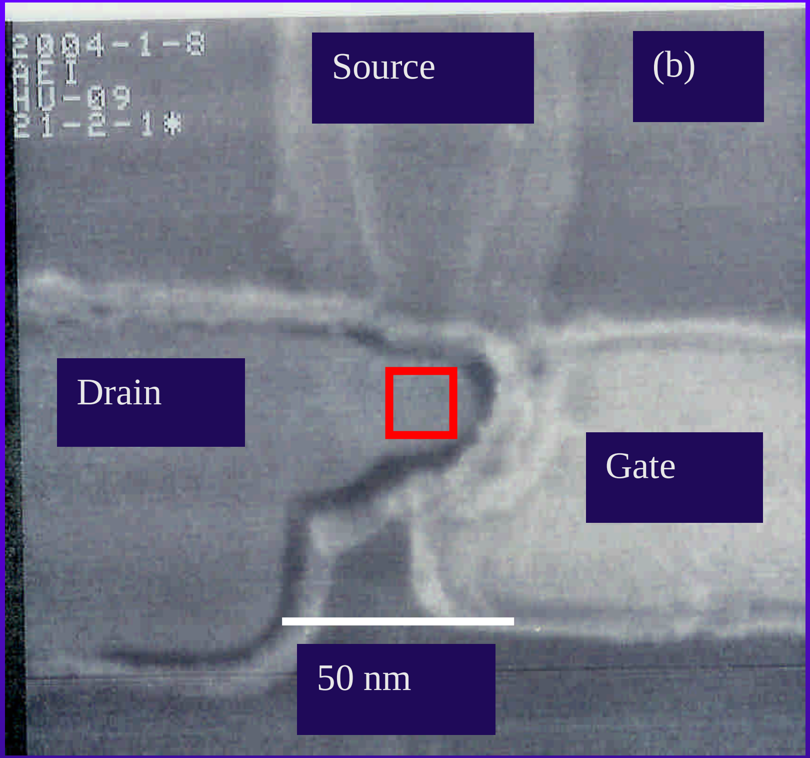


(c) Deposition 200 nm polysilicon (*in-situ* phosphorous) ,and Defined drain region of 20 nm width.



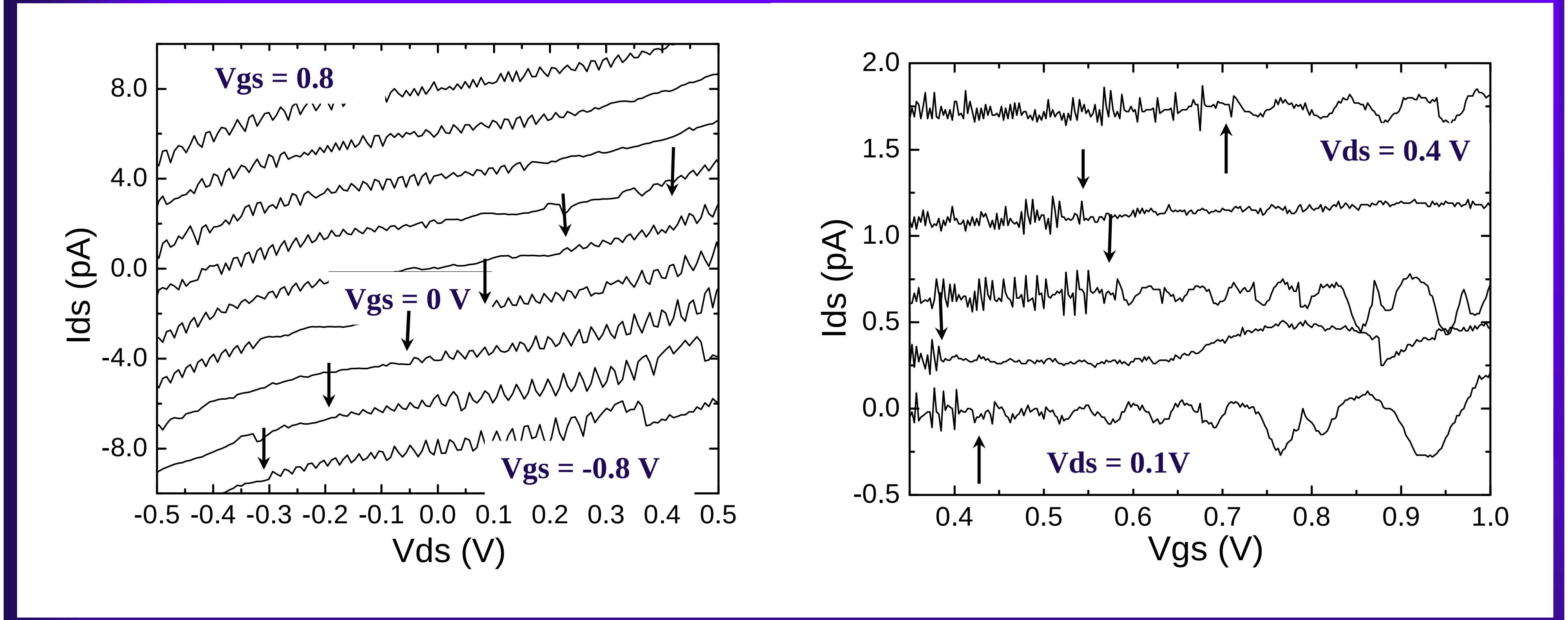
(3) mask3 by In-Line SEM

10x10x3nm^3 dot



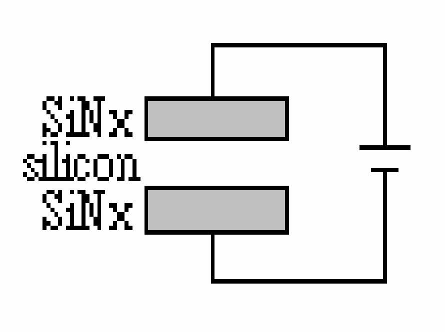
6 nm SiO_2 gate oxide, metal layer 300 nm.

I-Vs



Y. M. Wan et al. APL 87, 123506 (2005)

Single-electron charging



$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} = 3.5aF$$

$$\varepsilon_0 = 8.85 \times 10^{-12} (C^2 / Nm^2), \varepsilon_r = 11.7$$

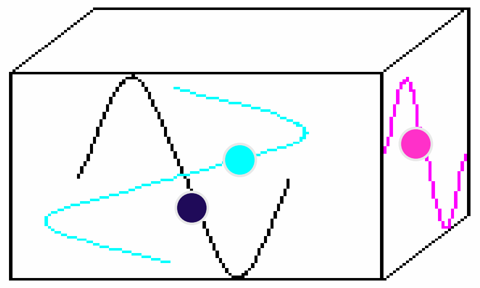
$$A = 10^{-16} (nm^2), d = 3(nm)$$

$$E_c = \frac{e^2}{2C_\Sigma} \approx 25(meV)$$

Onset states & charges

- Single-particle model in a box

$$E(n_x,n_y,n_z)=\frac{\hbar^2\pi^2}{2m}\left(\frac{n_x^2}{L^2}+\frac{n_y^2}{W^2}+\frac{n_z^2}{H^2}\right)$$

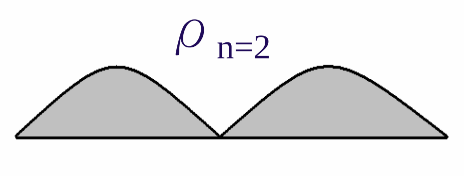


❖Coupling strength 220 mV/400 mV ～ 0.6

❖Gate-dot Cg = αC_Σ = 1.7aF

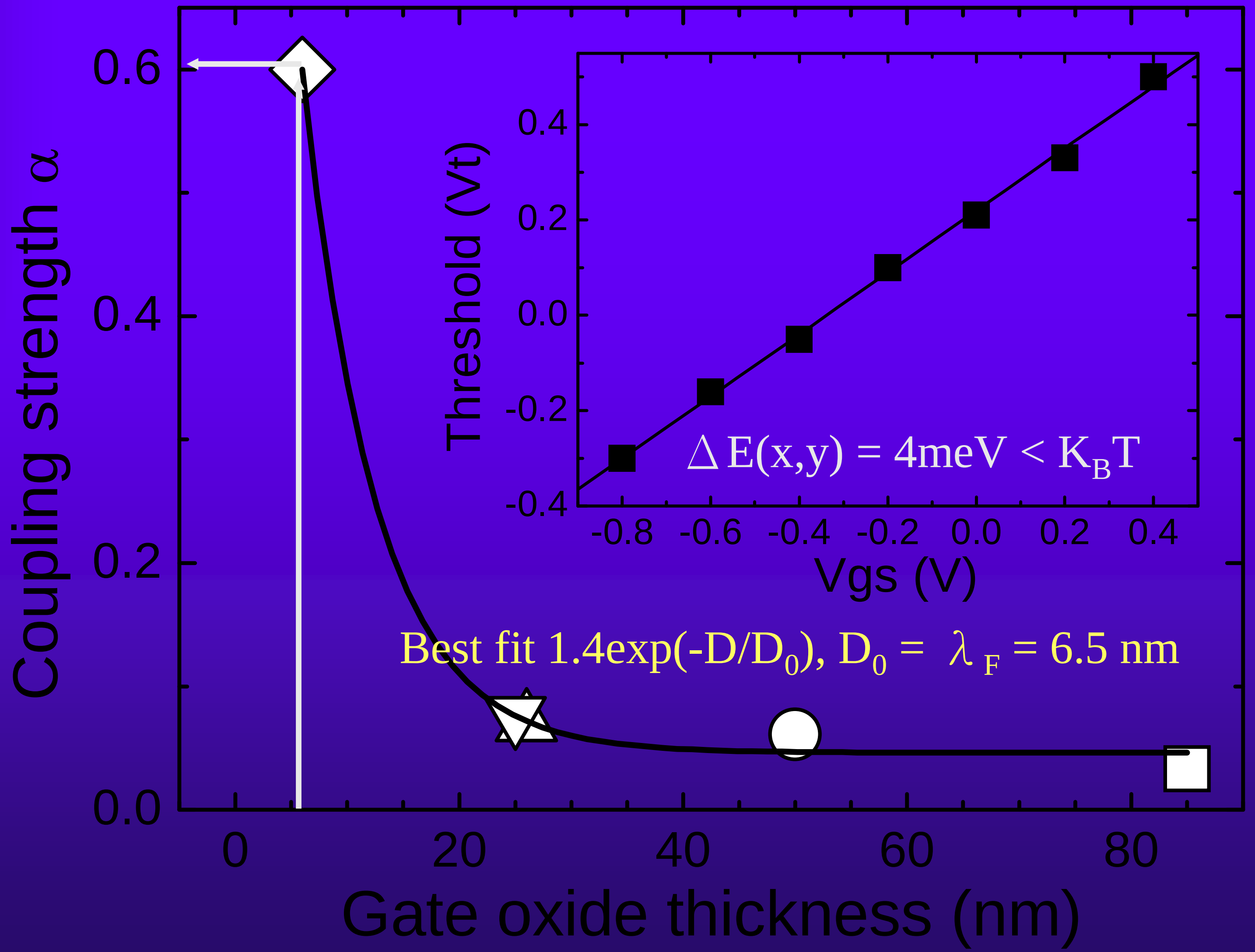
❖ ΔVgCg = e for Vgs > 0.7 V and ΔVg = 0.09V

❖ The onset voltage ～ 220 meV correspond to doublet of [2,3,2] and [3,2,2].



$$\rho_n(x,y,z)=\psi_n\psi_n^*$$

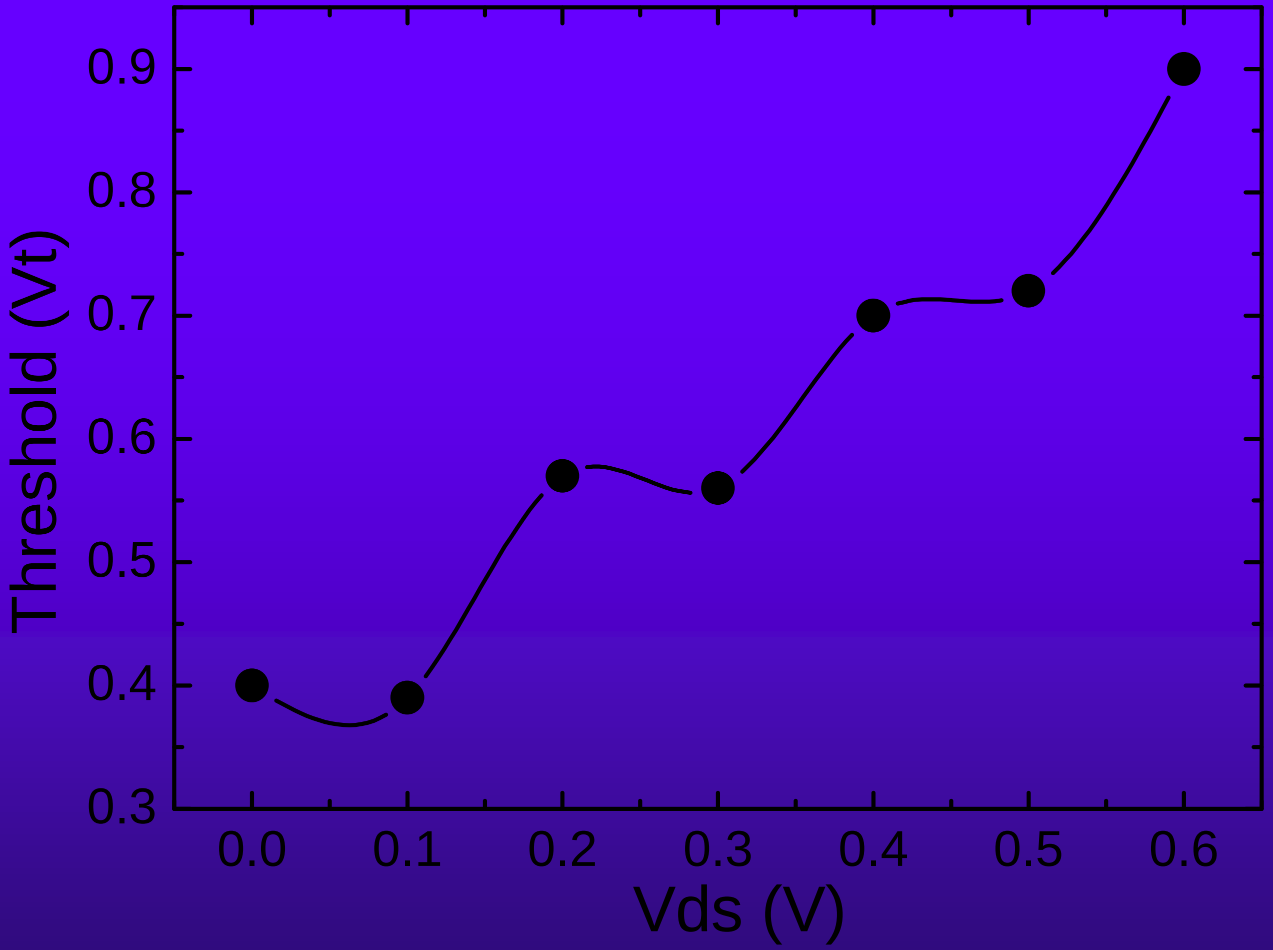
α vs oxide thickness



Best fit $1.4\exp(-D/D_0)$, $D_0 = \lambda_F = 6.5$ nm

【1】 Y. T. Tan et al. J. Appl. Phys. 94, 633, 2003.
【2】 M. Saitoh and T. Hiramoto. J. Appl. Phys, 91, 6725, *2002*
【3】 L. Zhuang et al., Appl. Phys. Lett. 72, 1205, 1998.

Threshold vs Vds



Modulation is observed because ΔEz= 40 meV > K_BT !

Summary for single-dot SET

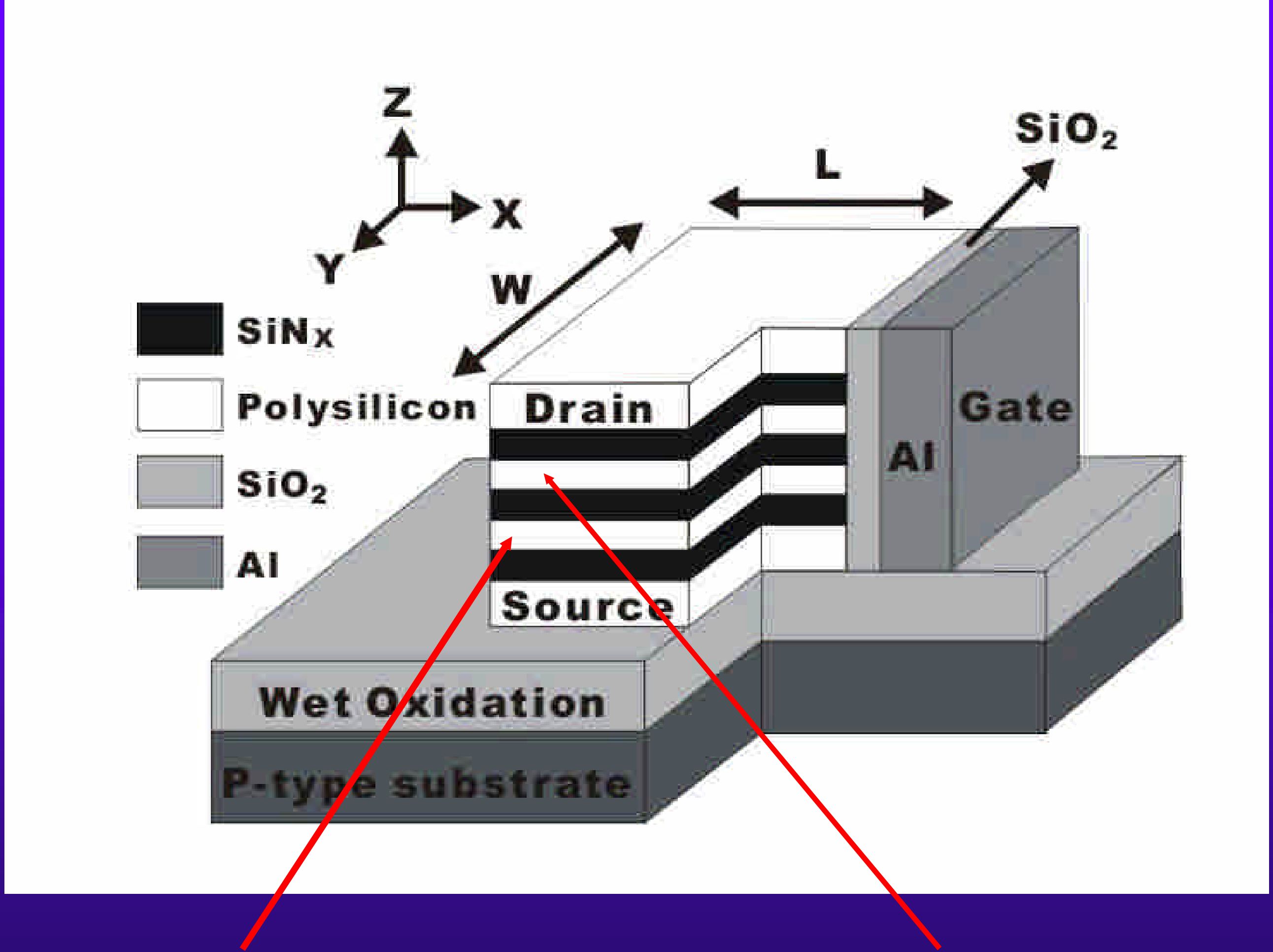
➢1. A new kind SET of SiNx/Si/SiNx nanopillars has been made.

➢2. I-V measurements at 300K show clear single-electron tunneling and side gate modulation.

➢3. The combination of co-plane and vertical transistors can be very useful in future applications.

➢4. The mixture of n=2 and n=3 states/charges at onset appears to be interesting and important.

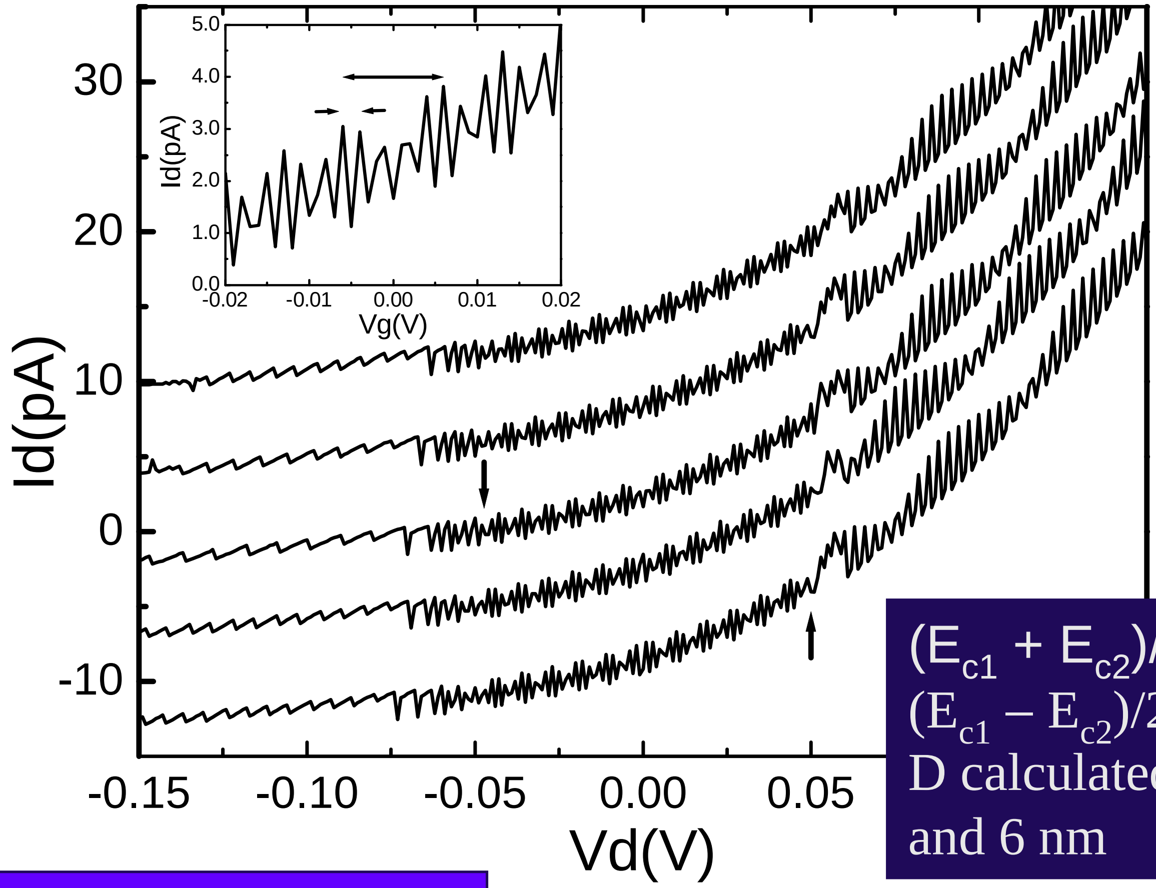
Double-dot Transistor



- SiNx(3-nm)-Si(3-nm)-SiNx(4.5-nm)-Si(1.5-nm)-SiNx(3-nm)

$\lambda_F \sim 9$ nm

Interference of carriers at n =1

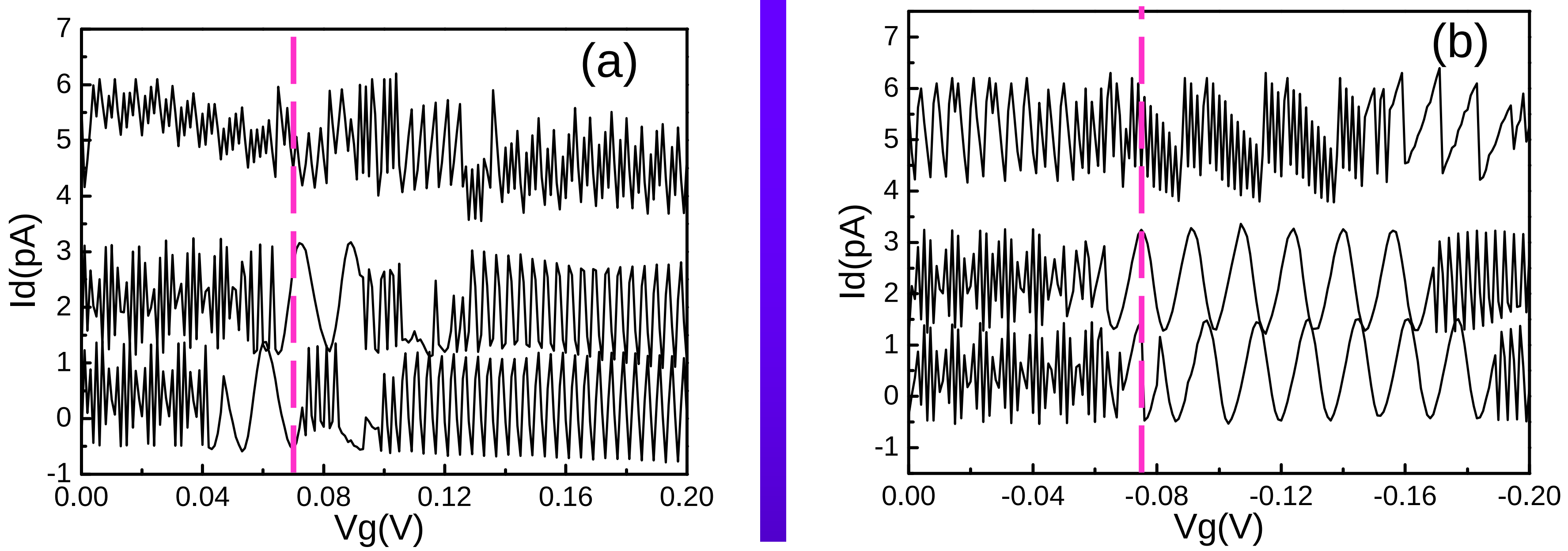


$(E_{c1} + E_{c2})/2 = 10$ meV
$(E_{c1} - E_{c2})/2 = 3.5$ meV
D calculated are 3 nm and 6 nm

Note: D is doubled !

Y. M. Wan et al. APL, 053515 (2006)

Single-electron tunneling at n ≥ 2



Vds = 0, 20 and 40 mV

- ❖ Side-gate charging onset at ∼ ± 65 meV
- ❖10 meV/15 meV = $\alpha \sim 0.67$ →gate oxide ~ 6 nm. $C_{dot} = C_{dot1} + C_{dot2} = 7.8$ aF, $C_g = \alpha C_{dot} \sim 5.2$ aF
- ❖$C_{\Sigma} = 3C_N + 2C_{dot} + C_g \sim 17$ aF and Ec = ~ 5 meV

Charging to easy spot

❖ L = H = W = 9 nm

[nx,ny,nz]	En(meV)
[1,1,1]	8.79
[2,2,2]	41
[2,2,3][2,3,2][3,2,2]	50
[3,2,3][2,3,3][3,3,2]	64.5

❖ Ec ∝ D

Material		Capacitor (aF)	Ec(meV)
Drain Nitride	C_d	1.86aF	43
Source Nitride	C_s	1.86aF	43
Center Nitride	C_c	1.24aF	56
Silicon dot(1)	C_{dot1}	2.6aF	30
Silicon dot(2)	C_{dot2}	5.18aF	15.4
Gate Oxide	C_g	1.72aF	46.5

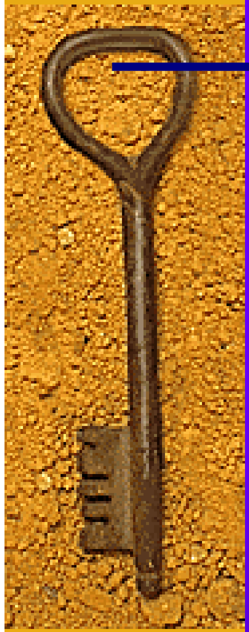
❖Forward charging correspond to the triplet [2,3,2] , [3,2,2] and [3,2,2].

❖Side charging reveals the triplet [3,3,2] , [3,3,2] and [3,2,3].

Conclusions

- Nanopillars' transistor appears to be a very promising candidate for 300 K applications.
- Interference of charge carrier at n=1 in a double-dot transistor is demonstrated.
- The mixture of n =2 and 3 at onset should be the key to understand the mechanism of resonance tunneling.
- We are working on a dynamical model for it.

Thanks to



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